MODELING OF LATTICE THERMAL EXPANSION FOR SIMULATION OF THERMAL STRESS IN 3D NANO MOSFETS

Abderrazzak El Boukili

Al Akhawayn University in Ifrane, Morocco

Email: a.elboukili@aui.ma

ABSTRACT

We are developing new model to calculate the lattice thermal expansion coefficient of Silicon Germanium (Si(1-x)Ge(x)) thin films used as performance boosters for nanoscale PMOSFETs. These models take into account the dependence of thermal expansion coefficient on Germanium mole fraction x and temperature. This thermal expansion coefficient is used to calculate the thermal induced intrinsic stress in Si(1-x)Ge(x) thin film after deposition. And this intrinsic stress is used to calculate and simulate numerically the resulting extrinsic stress in the channel of a nano PMOS based on Intel technology. 3D simulation results of channel stress will be presented, analyzed, and compared with literature.

Keywords: lattice thermal expansion coefficients, 3D modeling and simulation, thermal induced stress, Intel nano PMOSFETs

1. INTRODUCTION

Most of nano semiconductor device manufacturers as Intel, IBM and TSMC are intentionally using the intrinsic stress σ_0 to produce uniaxial extrinsic stress σ in the Silicon channel of nano MOSFETs. And, it is now admitted that the channel stress enhances carrier mobilities for both nano PMOS and NMOS transistors (Chui 2007; Bera 2006; Krivokapic 2003). This mobility enhancement fundamentally results from alteration of electronic band structure of silicon due to extrinsic stress. The extrinsic stress is the stress that exits in the whole transistor to balance the intrinsic stress that exists in different materials (or films) that make up the transistor. The intrinsic stress is either introduced intentionally or unintentionally or both. The unintentional intrinsic stress is induced by the processing steps as: implantation, etching, deposition of thin films, oxidation, shallow trench isolation, doping, diffusion, dislocation loops, or capping layers. The intentional intrinsic stress is introduced intentionally by the manufacturers to increase performance. Intel technology is using compressed Si(1-x)Ge(x) pockets in source and drain of nano PMOSFETs to introduce a compressive uniaxial extrinsic stress σ in the channel. This compressive stress σ has the advantage of enhancing the mobility of holes. Consequently, this will enhance the electrical performances of the nano PMOS devices by 30% or more (Chui 2007, Ghani 2003). This extrinsic stress σ is due to an intrinsic stress σ_0 that is generated in Si(1-x)Ge(x) films after deposition. And, this intrinsic stress σ_0 is due mainly to material mismatch or thermal mismatch. In this paper, we are focusing mainly on developing new analytical models for the thermal expansion coefficients $\alpha_{Si(1-x)Ge(x)}(T)$ of Si(1-x)Ge(x) film and $\alpha_{Si}(T)$ of the Silicon (Si) substrate. Here T represents the deposition temperature. It could also represent the diffusion temperature. These models take into account the dependence of thermal expansion coefficients (TECs) on the Germanium mole fraction x and the temperature. These coefficients are used to calculate accurately the intrinsic stress σ_0 due to thermal mismatch between the Si substrate and the Si(1-x)Ge(x) film. The 3D simulations and analysis of the resulting extrinsic stress σ will also be presented. The equations relating σ_0 and σ will be presented in Section 3. The intrinsic stress σ_0 due to thermal mismatch is caused by the different thermal expansion coefficients of the thin film Si(1-x)Ge(x) and the Silicon substrate. In fact, the temperature is high during deposition of Si(1-x)Ge(x) films. And, the temperature will cool down to room temperature after deposition. Then, a compressive intrinsic stress σ_0 will develop in the thin film and in the substrate during the cooling down to room temperature. We are going to neglect the intrinsic stress in the Si substrate since Si substrate is thick. Thermal expansion coefficients $\alpha_{Si(1-x)Ge(x)}(T)$ or $\alpha_{Si}(T)$ are, in general, extremely important for the performance of semiconductor devices as MOSFETs, bipolar transistors, laser diodes, solar cells, or micro-electromechanical systems (MEMS). This is because they create stress at the interface between the film and

the substrate during deposition, diffusion, etching, oxidation, doping, or any other processing step. And, this stress can affect significantly the performance. Thermal expansion coefficients of different semiconductor materials have been the focus of many researchers in the last decays. They have been studied both experimentally (Reeber 2000; Toshimaro 2002; Giles 2005; Okada 1984) and theoretically (Berrardi 1996; Xu 1992; Talwer 1995; Xie 1999). However, even for the same material such as Diamond (Toshimaro 2002, Giles 2005), Silicon (Okada 1984) and Gallium Nitride (Reeber 2000, Roder 2005) the available experimental data scattered significantly depending on the measuring methods. The main objective of this paper is to develop new analytical models based on polynomials for the temperature dependent TECs. These models are simple, and easy to fit with experiments compared to those found in literature (Garai 2007; Reeber 2000; Toshimaro 2002; Okada 1984; Xu 1992; Bruls 2001; Reeber 1975; Debernardi 2001). The scientific evidence of the simplicity of the proposed polynomial models is shown in the equations (2) and (3). The four unknowns in the equations (2) and (3) are easily and exactly calculated by using the equations (4) or (5) and a simple Gauss-Jordan elimination method for a dense matrix. Some researchers have used the *ab initio* method to calculate the temperature dependent TECs for Al (Debernardi 2001). But, this method involves the bulk modulus, mode Grüneisen constant, and the concave parameter. These parameters are based on many physical assumptions that are not always valid and they are not easy to fit to experiments. This paper is organized as follows. Section 2 will outline the main sources of intrinsic stress in Si(1-x)Ge(x) films after deposition. Section 3 will present the new physically based models for thermal expansion coefficients of Si(1-x)Ge(x) films and Si substrate. It will also present the mathematical models we are using to calculate the initial stress σ_0 due to thermal mismatch, and the resulting extrinsic stress σ. Section 4 will present the 3D simulation results of the channel extrinsic stress σ. This section will also analyze qualitatively and quantitatively the numerical results and provide some comparisons with the results found in the literature. Section 5 presents the concluding thoughts and future work.

2. INITIAL STRESS SOURCES

The main processing step in determining the initial stress in Si(1-x)Ge(x) films is deposition. This processing step takes place at elevated temperatures. When the temperature is decreased, the volumes of the grains of Si(1-x)Ge(x) film shrink and the stresses in the material increase. The stress gradient and the average stress in the film depend mainly on the Germanium ratio x, the substrate temperature and orientation, and the deposition technique which is usually LPCVD (low pressure chemical vapor deposition) or PECVD (plasma enhanced chemical vapor deposition), or Epitaxy. The initial stress σ_0 existing in thin films after deposition is caused mainly by lattice mismatch and thermal mismatch.

2.1. Intrinsic stress due to lattice mismatch

During deposition, thin films are either stretched or compressed to fit the substrate on which they are deposited. After deposition, the film wants to be smaller if it was stretched earlier, thus creating tensile intrinsic stress. And similarly, it creates a compressive intrinsic stress if it was compressed during deposition. The intrinsic stress generated due to this phenomenon can be quantified by Stoney's equation which relates the stress to the substrate curvature or by other advanced models (El Boukili 2010).

2.2. Intrinsic stress due to thermal mismatch

Thermal mismatch stress occurs when two materials with different coefficients of thermal expansion are heated and expand or contract at different rates. During thermal processing, thin film materials like Si(1-x)Ge(x), Poly-Silicon, Silicon Dioxide, or Silicon Nitride expand and contract at different rates compared to the Silicon substrate according to their thermal expansion coefficients. This creates an intrinsic strain and stress in the film and also in the substrate. The thermal expansion coefficient is defined as the rate of change of strain with respect to temperature.

3. MODELING OF LATTICE THERMAL EXPANSION COEFFICIENTS AND THERMAL INDUCED INTRINSIC STRESS

From the point of view of classical thermodynamics and lattice quantum vibrations, the temperature dependent TECs are found analogous to the temperature dependent specific heat (Xie 1999; Roder 2005; Bruls 2001). Many researchers have used the model of specific heat based on exponential functions to derive different models for temperature dependence of TECs (Reeber 2000; Toshimaro 2002; Okada 1984; Xu 1992; Bruls 2001; Garai 2007; Reeber 1975; Debernardi 2001).

These models could reproduce the profile of measured temperature dependent TECs. But, they are based on many physical assumptions that are not always valid. And, they involve many physical parameters that should be fitted. Which make these models difficult to use in practice.

Some researchers have used the *ab initio* method to calculate the temperature dependent TECs for Al (Debernardi 2001). But, this method involves the bulk modulus, mode Grüneisen constant, and the concave parameter. These parameters are also not easy to fit to experiments.

Some researchers have used the phenomenological lattice dynamical theory in quasi-harmonic approximation to describe the temperature dependence of TECs (Xie 1999).

A deep understanding of the atomistic origin of the thermal expansion and the accurate modeling of TECs by an easy and physically based formula is still a

challenge.Experimentally, the temperature dependent TECs have been described by polynomials (Toshimaro 2002; Bruls 2001; Garai 2007).

The objective of this paper is to develop and analyze new analytical models based polynomials for the temperature dependent TECs. We are proposing the following models:

$$\alpha_{Si(1-x)Ge(x)}(T) = (1-x)\alpha_{Si}(T) + x\alpha_{Ge}(T), \quad (1)$$

where x is the Germanium mole fraction.

To take into account the temperature effects, we are proposing the following polynomials of degree two since most of observed TECs are nonlinear:

$$\alpha_{Si}(T) = T\,(a_{Si}T + b_{Si}) \quad (2)$$

$$\alpha_{Ge}(T) = T\,(a_{Ge}T + b_{Ge}) \quad (3)$$

The constants $a_{Si}, b_{Si}, a_{Ge}, b_{Ge}$ are calculated exactly using the following experimental models given for T = 300 K (Schaffler 2001):

If $(x < 0.85)$ then:

$$\alpha_{Si(1-x)Ge(x)}(300) = (2.6 + 2.55x) \times 10^{-6} \quad (4)$$

If $(x > 0.85)$ then:

$$\alpha_{Si(1-x)Ge(x)}(300) = (-0.89 + 7.53x) \times 10^{-6} \quad (5)$$

Now let's use the thermal expansion coefficients $\alpha_{Si(1-x)Ge(x)}(T)$ and $\alpha_{Si}(T)$ to model analytically the thermal induced intrinsic strain ε_0 and intrinsic stress σ_0.

The intrinsic strain tensor, ε_0, is defined by:

$$\varepsilon_0 = (\varepsilon_0^{xx}, \varepsilon_0^{yy}, \varepsilon_0^{zz}, \varepsilon_0^{xy}, \varepsilon_0^{yz}, \varepsilon_0^{xz}), \quad (6)$$

where $\varepsilon_0^{xx}, \varepsilon_0^{yy}, \varepsilon_0^{zz}$ are the intrinsic normal strain components, and $\varepsilon_0^{xy}, \varepsilon_0^{yz}, \varepsilon_0^{xz}$ are the intrinsic shear strain components. We assume that in Si(1-x)Ge(x):

$$\varepsilon_0^{xx} = \varepsilon_0^{yy} = \varepsilon_0^{zz} = \varepsilon^0_{SiGe}(T). \quad (7)$$

For simplicity, let:

$$\alpha_{Si(1-x)Ge(x)}(T) = \alpha_{SiGe}(T)$$

The thermal expansion coefficient of Si(1-x)Ge(x) is defined as the rate of change of the intrinsic strain component, $\varepsilon^0_{SiGe}(T)$, with respect to temperature T. Its unit is micro strain/Kelvin (με/K) and it is given by:

$$\alpha_{SiGe}(T) = \frac{d\,\varepsilon^0_{SiGe}(T)}{dT} \quad (8)$$

Then, the intrinsic strain component will be given by:

$$\varepsilon^0_{SiGe}(T) = -\int_{T_0}^{T} \alpha_{SiGe}(t)\,dt \quad (9)$$

where T0 is the ambient temperature and T is the processing temperature. For example, T could be the temperature during deposition of Si(1-x)Ge(x) thin film. The Si(1-x)Ge(x) film will cool down after deposition from T to T0. Then, it will contract. This explains the use the sign minus in the equation (9). We also assume that there is no thermal strain at room temperature T0.

On the other hand, to include the effects of the thermal expansion coefficient of the Si substrate, $\alpha_{Si}(T)$, on the intrinsic strain in Si(1-x)Ge(x) thin film, we add the term $\Delta\alpha(T)\Delta T$ to the model given by the equation (9). Then, the proposed model for the intrinsic strain component $\varepsilon^0_{SiGe}(T)$ is given by:

$$\varepsilon^0_{SiGe}(T) = \int_{T_0}^{T} \alpha_{SiGe}(t)\,dt + \Delta\alpha(T)\Delta T \quad (10)$$

where

$$\Delta\alpha(T) = \alpha_{SiGe}(T) - \alpha_{Si}(T), \quad (11)$$

$$\Delta T = T - T0. \quad (12)$$

The component form of the intrinsic stress, σ_0, is defined by:

$$\sigma_0 = (\sigma_0^{xx}, \sigma_0^{yy}, \sigma_0^{zz}, \sigma_0^{xy}, \sigma_0^{yz}, \sigma_0^{xz}),$$

where $\sigma_0^{xx}, \sigma_0^{yy}, \sigma_0^{zz}$ are the intrinsic normal stress components and $\sigma_0^{xy}, \sigma_0^{yz}, \sigma_0^{xz}$ are the intrinsic shear stress components that are also assumed to be zero. We also assume that in SiGe:

$$\sigma_0^{xx} = \sigma_0^{yy} = \sigma_0^{zz} = \sigma^0_{SiGe}(T). \quad (13)$$

On the other hand, we are using a physically based model to define the intrinsic stress tensor σ_0 in the Si(1-x)Ge(x) thin film, since, we are using the Hooke's elastic law to express the relation between strain and stress as follows:

$$\sigma_0 = D.\varepsilon_0, \quad (14)$$

In three dimensions, the stiffness tensor D, used in our model, for isotropic elastic materials as SiGe is given by:

$$D = \begin{bmatrix} c11 & c12 & c12 & 0 & 0 & 0 \\ c12 & c11 & c12 & 0 & 0 & 0 \\ c12 & c12 & c11 & 0 & 0 & 0 \\ 0 & 0 & 0 & c44 & 0 & 0 \\ 0 & 0 & 0 & 0 & c44 & 0 \\ 0 & 0 & 0 & 0 & 0 & c44 \end{bmatrix} \quad (15)$$

where the elastic constants c11,c12, and c44 for each material are depending on the Young modulus (E) and Poisson's ratio (γ). In this paper, we are taking into account the dependence of γ and E on the Germanium mole fraction and substrate orientations.

In our simulation program, the intrinsic stress tensor σ_0 is used as a source term to calculate, in the whole 3D nano MOSFET structure, the extrinsic stress tensor $\sigma = (\sigma^{xx}, \sigma^{yy}, \sigma^{zz}, \sigma^{xy}, \sigma^{yz}, \sigma^{zx})$. We note that σ^{xx}, σ^{yy}, and σ^{zz} represent the extrinsic stress along the channel, vertical to the channel, and across the channel. This channel stress is used to enhance the mobility of holes in 3D nano PMOSFETs based on Intel technology (Ghani 2003). We assume that Silicon and Silicon Germanium are elastic materials. And, to calculate the stress tensor σ we use the elastic stress model based on Newton's second law of motion, and the following Hooke's law relating stress to strain:

$$\sigma = D(\varepsilon - \varepsilon_0) + \sigma_{00} \quad (16)$$

Here σ_{00} is taken to be zero for simplicity. And, the components of ε_0 are given by the equation (6). A detailed description and how to use finite volume method to solve numerically the elastic model (16) in 3D is given in (El Boukili 2010).

4. 3D NUMERICAL RESULTS AND ANALYSIS

The third order model of intrinsic stress σ_0 is based on the proposed second order model of the thermal expansion coefficients $\alpha_{Si(1-x)Ge(x)}(T)$ and $\alpha_{Si}(T)$.

4.1 Validation of the proposed models for TECs using experimental values

For 300°K , the values of thermal expansion coefficients obtained from the proposed models for Si, Ge, and Si(1-x)Ge(x) are in excellent agreement with the values obtained from experiments. The developed models for Si and Ge are given by:

$$\alpha_{Si}(T) = (3.02e^{-10}T^2 - 8.19e^{-8}T)$$

$$\alpha_{Ge}(T) = (5.72e^{-12}T^2 + 3.13e^{-23}T)$$

If we take T=300°K, we find out that:

$$\alpha_{Si}(300) = 2.6e^{-6},$$

$$\alpha_{Ge}(300) = 5.15e^{-6},$$

The experimental values (Sze 1981) for T=300°K are:

$$\alpha_{Si}(300) = 2.6e^{-6},$$

$$\alpha_{Ge}(300) = 5.8e^{-6}.$$

We could then see that the values we get from the proposed models are exactly the same for Silicon and very close for Germanium. The following table (Table 1) shows the values of the TECs for different Germanium model fractions for Si(1-x)Ge(x) at T=300°K that we get from the proposed models and from experiments (Sze 1981).

Table 1: Comparison of Si(1-x)Ge(x) TECs

Germanium mole fraction	Proposed TECs	Experimental TECs
0.25	3.23e-6	3.4e-6
0.50	3.87e-6	4.2e-6
0.75	4.51e-6	5e-6

From this table, we should notice that the values of the proposed TECs are in good agreement with those given by experiments (Sze 1981). Another important point from Table 1 is that the values of the proposed TECs are increasing with Ge mole fraction as those obtained from experiments. The following table (Table 2) shows the behavior of the proposed TEC of Si(1-x)Ge(x)(T) for different temperatures at x=0.17.

Table 2: Proposed Si(.83)Ge(.17) TEC as function of temperature

Temperature T in °K	$\alpha_{Si(.83)Ge(.17)}(T)$
300	3.16e-6
400	1.44e-5
500	3.11e-5
600	5.29e-5
700	8e-5
800	1.12e-4
900	1.49e-4

1000	1.92e-4

From the Table 2, the TEC of Si(0.83)Ge(0.17)(T) is increasing with temperature. The same thing is valid for the TECs of Si and Ge since they are polynomials. Then, we could use the proposed models to predict the TECs of Si, Ge, and SiGe for high temperatures. Some models found in literature can predict reasonably the TECs of these materials only at low temperatures. And, for temperatures greater than Debye temperature (θ_D) these models fail.

4.2 Validation of the proposed TECs models using the numerically calculated channel stress

The intrinsic stress σ_0 is used to simulate numerically the 3D extrinsic stress σ in the channel of an Intel 45 nm gate length PMOSFET shown in Figure 1. For the following numerical results, we used (001) for the substrate orientation and 17% as the Germanium mole fraction. The results in Figures 2 and 3 show the 3D distribution of stress components along channel for 300°C and 1000°C respectively. A similar stress distribution has been reported in (Victor 2004) for a similar structure. The values of the calculated 3D extrinsic stress are also qualitatively and quantitatively in good agreement with those calculated in (Victor 2004). Figure 4 shows the contour lines of the stress component in x direction at 300°C. All these results did show that the processing temperatures have significant effects on intrinsic and extrinsic stress profiles. These temperature effects will also affect the performances of the MOSFETs devices. On the other hand, these numerical results confirm that the proposed models for thermal expansion coefficients $\alpha_{Si(1-x)Ge(x)}(T)$ and $\alpha_{Si}(T)$ provide valid and correct results for the extrinsic stress σ in 3D. We also believe that these results are of great interest to the semiconductor community including manufacturers as Intel, IBM, TSMC, and academia.

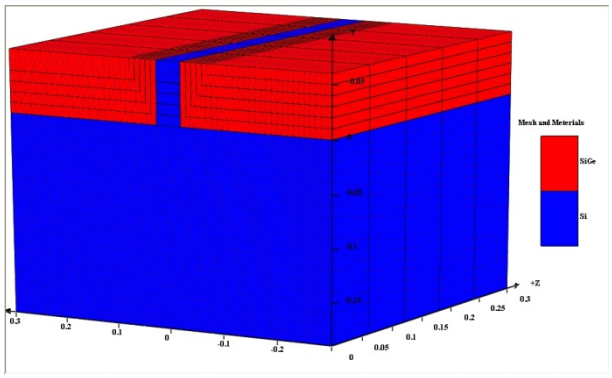

Figure 1: Materials and Mesh of The Simulated Structure

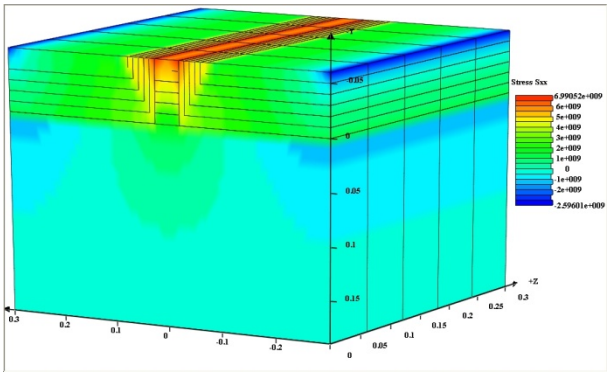

Figure 2: 3D Distribution of Stress Component Along Channel at 300°C

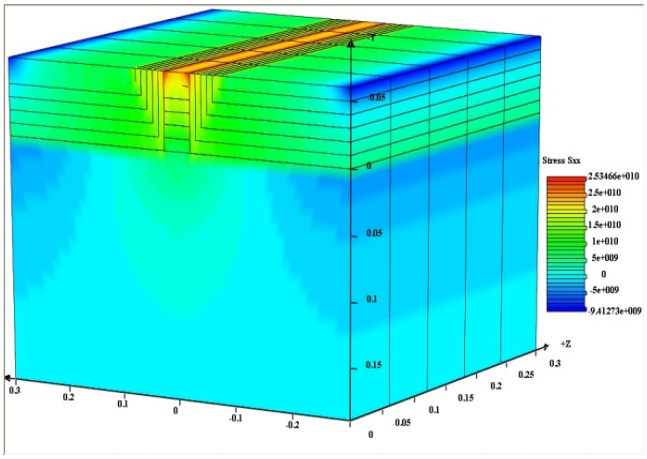

Figure 3: 3D Distribution of Stress Component Along Channel at 1000°C

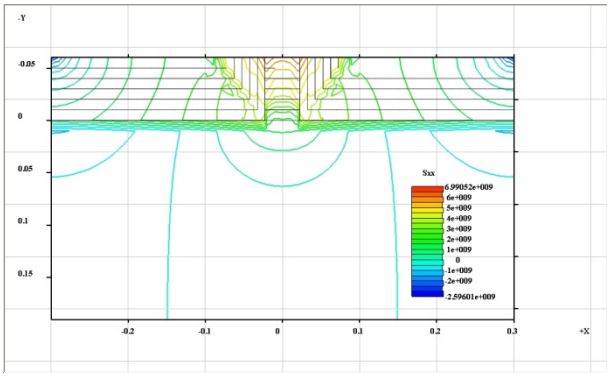

Figure 4: Contour Lines of Stress Component Along Channel at 300°C

5. CONCLUSIONS

In this paper, we have developed new second order models for the thermal expansion coefficients $\alpha_{Si(1-x)Ge(x)}(T)$ and $\alpha_{Si}(T)$. The results we got from these models for TECs of Si, Ge, and SiGe are in excellent agreement with experiments. And, we have used these models to calculate accurately and analytically the intrinsic stress σ_0 due to thermal mismatch after deposition. We have used the intrinsic

stress σ_0 to calculate numerically the resulting extrinsic stress σ in the channel of the Intel 45 nm PMOSFET shown in Figure 1. The numerical results we have got for σ are also in good agreement, qualitatively and quantitatively, with those found in the literature for a similar structure (Victor 2004). In the future, we will apply these models to predict the TECs of other semiconductor materials and metals.

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AUTHOR'S BIOGRAPHY

Abderrazzak El Boukili received both the PhD degree in Applied Mathematics in 1995, and the MSc degree in Numerical Analysis, Scientific Computing and Nonlinear Analysis in 1991 at Pierre et Marie Curie University in Paris-France. He received the BSc degree in Applied Mathematics and Computer Science at Picardie University in Amiens-France. In 1996 he had an industrial Post-Doctoral position at Thomson-LCR company in Orsay-France where he worked as software engineer on Drift-Diffusion model to simulate hetero junction bipolar transistors for radar applications. In 1997, he had European Post-Doctoral position at University of Pavia-Italy where he worked as research engineer on software development for simulation and modeling of quantum effects in hetero junction bipolar transistors for mobile phones and high frequency applications. In 2000, he was Assistant Professor and Research Engineer at the University of Ottawa-Canada. Through 2001-2002 he was working at Silvaco Software Inc. in Santa Clara, California-USA as Senior Software Developer on mathematical modeling and simulations of vertical cavity surface emitting lasers. Between 2002-2008, he was working at Crosslight Software Inc. in Vancouver-Canada as Senior Software Developer on 3D Process simulation and Modeling. Since Fall 2008, he is working as Assistant Professor of Applied Mathematics at Al Akhawayn University in Ifrane-Morocco. His main research interests are in industrial TCAD software development for simulations and modeling of opto-electronic devices and processes.
http://www.aui.ma/personal/~A.Elboukili.